Electric Druid ADSR Envelope Generator

Introduction

This voltage-controlled ADSR envelope generator chip is a completely modern, microprocessor-based design that emulates the analogue ADSR chips of the late 70's and 80's.

The two key chips that were used as a model are the CEM3312 Voltage Controlled Envelope Generator and the SSM2056 Voltage Controlled Envelope Generator. The first of these was used in the Sequential Pro-One (and probably many other Sequential synths) and the SSM was used in the Korg Polysix, amongst others. In many ways these are extremely similar ICs. Both chips include control voltages for A, D, S and R.

The CEM3312 includes a CV pin for the final envelope output level. This is intended to provide a voltage-controlled envelope depth to a VCF in programmable systems. As such, this is a very useful feature, and saves a VCA doing the job, as they point out in the datasheet. It can also be used to provide velocity sensitivity if fed a velocity CV.

The SSM2056 includes a pin for the keyboard CV. An increasing voltage on this pin reduces the attack, decay, and release times overall. This allows you to set up shorter envelopes at the high end of the keyboard than the low end, mimicking the effect of many natural percussion instruments.

This VCADSR chip includes both these inputs, LEVEL CV and TIME CV. It also includes a digital input to select between the 'traditional' exponential envelope shape and a linear envelope, typical of early-era digital synths.

The output from the chip is a PWM pulse train which only requires simple lowpass filtering to produce a genuine ADSR envelope shape.

Features

Range of around 1 mSec to 10 Sec.

The Minimoog, Sequential Pro-One and SH101 all have a famously quick attack time. I've never measured it, but it's supposed to be around 1 mSec. This envelope generator can also produce times that short.

Most analogue synths can do a slow attack of a handful of seconds, but 10 seconds gives a neat range of 1:10000 to be covered by the control voltages, and allows really slowly evolving sounds to be generated.

8-bit resolution on the control voltages

The Sequential Prophet 5 used a 7-bit control resolution, so this is going slightly better. Whether a standard potentiometer actually has the accuracy to directly produce 8 bit resolution is another question.

10 bit envelope output resolution

The internal envelope mapping and calculation is 8-bit, but the final LEVEL_CV multiplication provides a 16-bit output, of which 10 bits are fed to the PWM module.

19.5KHz sample output rate

The PWM frequency is around 19.5KHz. This allows the PWM output to be heavily filtered for a smooth analogue output whilst maintaining the snappy response. The two-stage 24dB Bessel filter provides the best-possible pulse filtering.

Logarithmic time control response over 1:10,000 range

The A, D and R control voltage inputs give the full range from 1 mSec to 10 Secs in four even decades, eg 1-10mSecs, 10-100mSecs, 100-1000mSecs, and 1-10Secs. Since the response of the CV inputs is logarithmic, this is possible with simple linear potentiometers.

Separate gate and trigger inputs

The chip has separate GATE and TRIGGER inputs, which allows the envelope to be retriggered whilst the gate is still high. For GATE-only operation, these inputs can be tied together with an RC highpass filter - see page 5.

Exponential and Linear Envelopes

The chip can produce classic exponential ADSR curves suitable for volume control with a linear VCA, or can produce linear envelopes typical of early digital synths. These can be more suitable for use with exponential VCAs.

Pinout Diagram

PIC16F684
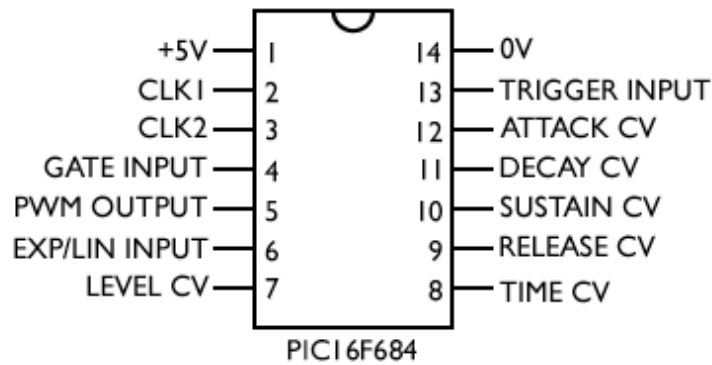
| Pin	Function	Details	Notes
1	+5V	Power supply	
2	CLK1	Connect to Xtal	20MHz Clock
3	CLK2	Connect to Xtal	20MHz Clock
4	GATE INPUT	0-5V digital input	Envelope goes to RELEASE stage on falling edge of 0-5V pulse.
5	PWM OUTPUT	0-5V digital output	PWM output at 19.5KHz
6	EXP/LIN INPUT	0-5V digital input	0V - Exponential envelope 5V - Linear envelope
7	LEVEL CV	0-5V analogue input	8 bit, values from 0 to 255
8	TIME CV	0-5V analogue input	8 bit, values from 0 to 255
9	RELEASE CV	0-5V analogue input	8 bit, values from 0 to 255
10	SUSTAIN CV	0-5V analogue input	8 bit, values from 0 to 255
11	DECAY CV	0-5V analogue input	8 bit, values from 0 to 255
12	ATTACK CV	0-5V analogue input	8 bit, values from 0 to 255
13	TRIGGER INPUT	0-5V digital input	Envelope goes to ATTACK stage on rising edge of 0-5V pulse.
14	0V	Power supply	

Application Notes

Basic circuit diagram
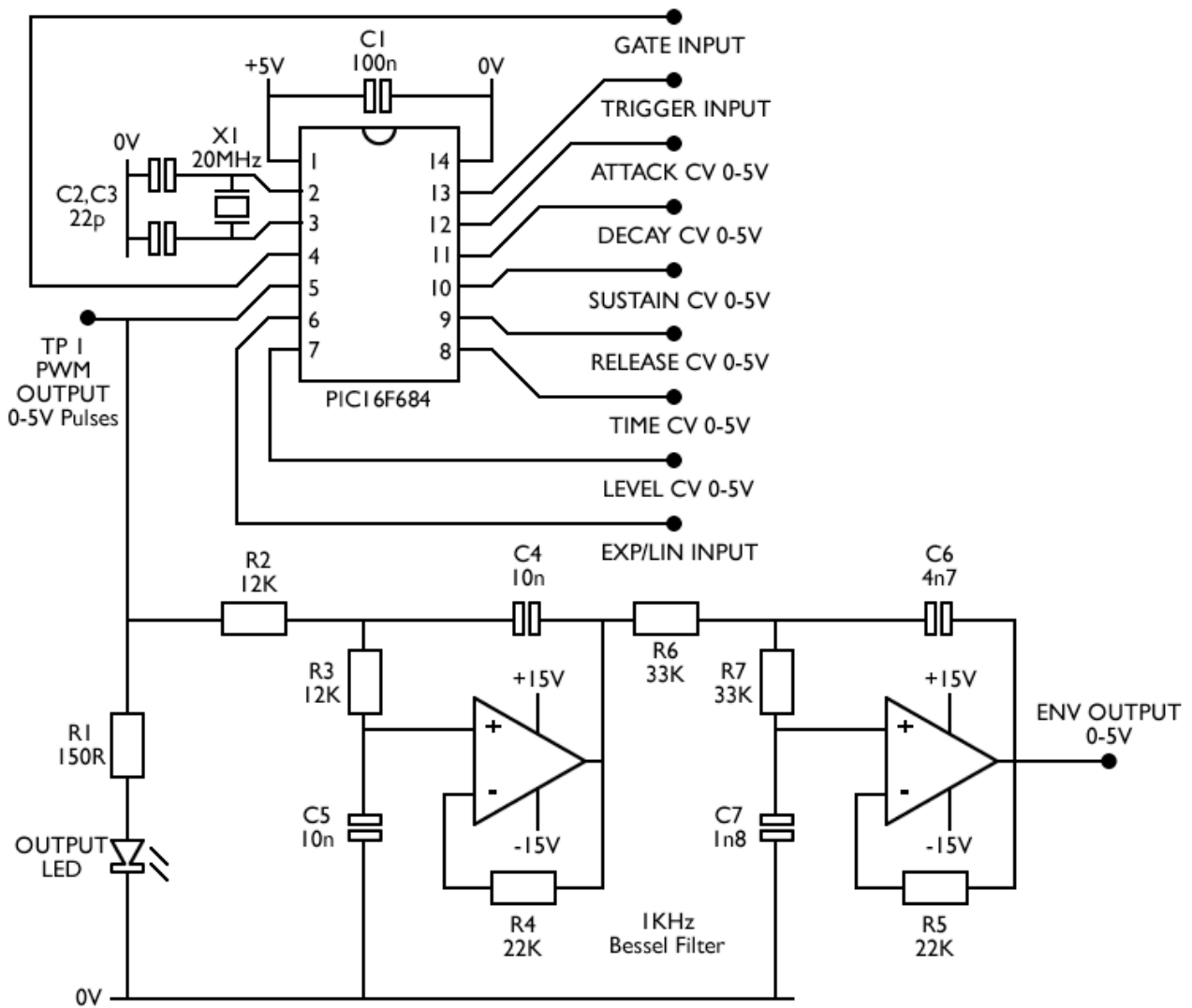
Using potentiometers for CVs

The required control voltages can be generated directly by potentiometers as follows, or by a microprocessor driving a DAC in a programmable system.
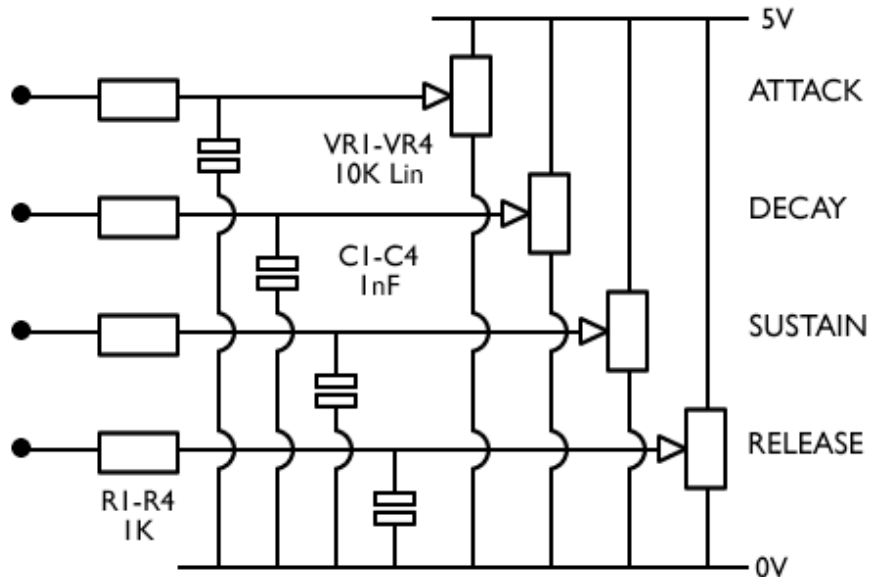
Disabling unwanted inputs

If not required, TIME CV should be connected to 0V via 1K. LEVEL CV can be disabled by connecting to +5V with a 1K resistor. If linear envelopes are not required, tie EXP/LIN to 0V with a 10K resistor.

Using the chip with GATE only

For GATE only use, the TRIGGER input can simply be connected directly to the GATE input. Since only the TRIGGER responds to the leading edge of the pulse (starting the ATTACK stage), and only the GATE responds to the falling edge (starting the RELEASE stage), there is no problem. If an optional TRIGGER jack input is required, it can be connected to GATE with a normalled jack connection.