SSI2140

FATKEYS™ VOLTAGE CONTROLLED MULTI-MODE FILTER

The SSI2140 is a new-generation voltage controlled filter that provides four highly-configurable variable transconductance cells for a wide variety of pole and mode combinations, and adds significant new features.

Based on an updated core by SSM2040 designer Dave Rossum, the SSI2140 temperature compensates its transconductance cells for unprecendented stability. Temperature compensation is also optionally available for the exponential control.

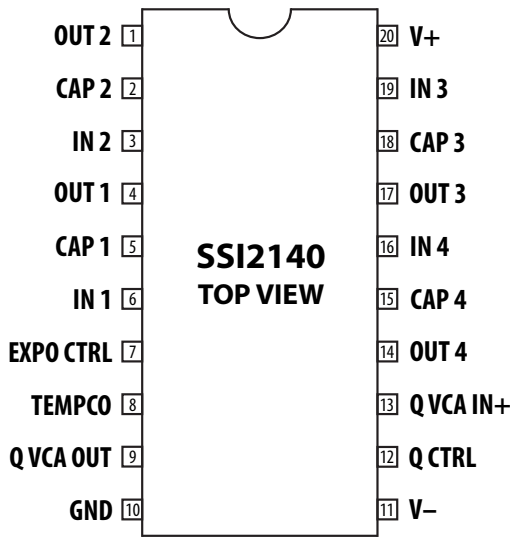
A temperature compensated VCA with linear control allows easy control of resonance and supports multiple Q compensation schemes, or otherwise used for traditional VCA/VCF roles.

Virtually any type of filter response from one to four poles can be achieved including low-pass, high-pass, band-pass, all-pass, notch, Sallen & Key, biquad, Cauer, state-variable, and others.

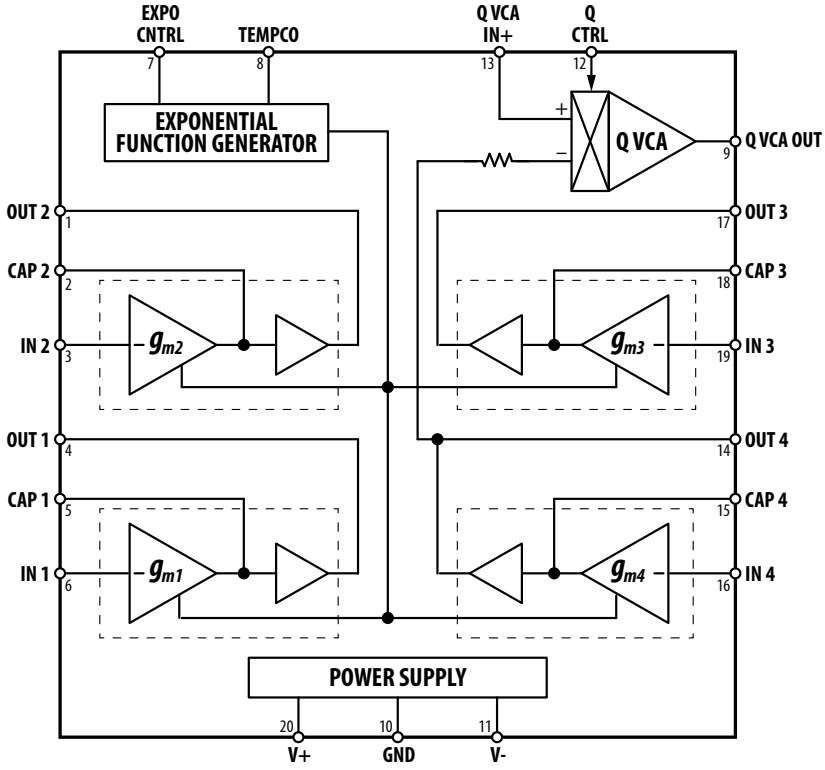
Most importantly, great care was taken to preserve the SSM2040's sonics including an input stage that can be overdriven for classic analog synthesizer character.

FEATURES

- **Highly Configurable Four-Section Filter**
- **Preserves SSM2040's Classic Filter Sound**
- **Exponential Frequency Control, with Optional Temperature Compensation**
- **On-Chip Resonance Circuit with Linear Control**
- **Multiple Q Compensation Schemes**
- **±4V to ±16V Operation**
- **Ultra-Compact 20-Lead SSOP Package**



PIN CONNECTIONS
20-LEAD SSOP



FUNCTIONAL BLOCK DIAGRAM

The SSI2140 is available exclusively from Sound Semiconductor and its authorized resellers

PO Box 1587, Arroyo Grande, CA 93421 USA, www.soundsemiconductor.com

Rev. 3.1.1, March 2023

SPECIFICATIONS (V_S = ±12V, f = 1kHz, V_{IN} = V_{EXPO} = V_Q = GND, I_Q = 0µA, T_A = 25°C; using Figure 1 and 3 circuits unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
POWER SUPPLY						
Supply Voltage Range	V_S		±4		±16	V
Supply Current	I_S		±3.5	±4.8	±6.5	mA
EXPO FUNCTION GENERATOR						
Frequency Control Sensitivity				-18.4		mV/oct
Frequency Control Input Range		Fully open to fully closed	-100		+300	mV
Frequency Control Input Bias Current				90		nA
Control Feedthrough		See Note 1		-66		dB
Exponential Scale Factor Drift						
Tempco Enabled				+700		ppm/°C
Tempco Disabled				-3250		ppm/°C
Tempco Resistor Nominal Value			830	890	950	Ω
Tempco Resistor Temp. Coefficient				+3950		ppm/°C
TRANSCONDUCTANCE CELLS						
Transconductance	g_m	V_{EXPO} = 0V	160	215	270	µS
		V_{EXPO} = -36mV	700	850	1000	µS
Input Offset Voltage, Each Cell			0	0.65	2.0	mV
Change in Offset Voltage, Four Cells in Series		±5 Octave Frequency Range		0.6		mV
Transconductance Temp. Coefficient				±200		ppm/°C
Input Bias Current		V_{EXPO} = 0V		50		nA
Buffer Output Sink Current				1.6		mA
Buffer Output Source Current				10		mA
Equivalent Input Noise, Each Cell	EIN	V_{EXPO} = -90mV, 20Hz–20kHz		0.5		$µV_{RMS}$
Passband Total Harmonic Distortion	THD	V_{IN} = $1V_{P-P}$, V_{EXPO} = -90mV		0.1		%
RESONANCE AND Q VCA						
Q Control Input Current Range	I_Q		0		500	µA
Q Control Current at Oscillation				222		µA
Q VCA Transconductance Coefficient	Kg_m			30		µS/µA
Q VCA Output Leakage				1.1		µA
Q VCA Input Bias Current		V_{CTRL} = 222µA		1.1	2.0	µA
Output Compliance			-0.3		V+ - 1.1	V

[1] V_{IN} = GND, I_Q = 0µA, with V_{EXPO} input ±18mV 1kHz sinewave at pin 7

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Current into any Signal Pin	±5mA
Max Voltage, any Pin (whichever is greater)	V- minus 0.3V V- plus 36V V+ plus 0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-40°C to +85°C
Lead Temperature (Soldering, 10 sec)	260°C

ORDERING INFORMATION

Part Number	Package Type/Container	Quantity
SSI2140SS-TU	20-Lead SSOP*, Tube Packing	76
SSI2140SS-RT	20-Lead SSOP*, Tape and Reel	2500
EVB2140LP-B	Evaluation Board, blank with SSI2140	1
EVB2140LP-P	Evaluation Board, fully assembled	1
DAB2140	SSI2140 SSOP to DIP Adapter	1

*SSI Package ID "**PSSL20**"
Mechanical drawing available at www.soundsemiconductor.com

PIN DESCRIPTIONS ("x" refers to one of the four transconductance sections)

Pin(s)	Name	Description
1, 4, 14, 17	OUT x	Output of transconductance cell buffer amplifier. Limited to ±1V swing, and can source 10mA and sink 1.6mA. 10kΩ or greater feedback and load resistors are recommended.
2, 5, 15, 18	CAP x	Integrating capacitor connected between CAP x and GND. To ensure stability, use values of 50pF or greater.
3, 6, 16, 19	IN x	Inverting input to variable transconductance amplifier. For optimum control rejection, the recommended input network is a 10kΩ input resistor with a 200Ω attenuating resistor to GND.
7	EXPO CTRL	Control voltage that sets gain of the four transconductance amplifiers. The control response is exponential, with typical sensitivity of -18mV/octave.
8	TEMPCO	Internal 890Ω (typical) temperature compensating resistor. If unused, leave disconnected.
9	Q VCA OUT	Output current of the Q VCA. If not used, connect to ground.
10	GND	Connect to analog signal ground with short, low inductance trace.
11	V–	Negative supply. Recommend 100nF local decoupling capacitor placed as close to package as possible with a low inductance trace to ground.
12	Q CTRL	Current control of Q VCA gain. Ground-referenced current input.
13	VCA IN+	Non-inverting input of the Q VCA. The inverting input is internally connected to OUT 4.
20	V+	Positive supply. Recommend 100nF local decoupling capacitor placed as close to package as possible with a low inductance trace to ground.

USING THE SSI2140

The SSI2140 contains four exponentially controlled transconductance cells ("g_m") with ultra-low bias current buffers. These cells and their associated buffers have been updated by the original designer to recreate audio characteristics of the acclaimed SSM2040 Voltage Controlled Filter, but include a few specific improvements:

- The buffer bias current has been decreased by an order of magnitude, providing improved frequency control voltage rejection.
- Transistor geometries have been optimized for superior noise performance.
- The control circuitry has been temperature compensated to minimize the change of each cell's g_m with die temperature variations.
- The transconductance at $V_{EXPO} = 0V$ for the SSI2140 may vary slightly from the SSM2040. The SSM2040 was specified at typically 200µS, with a production variation range of 3:1. The SSI2140 has a typical value of 215µS and production variation range of 1.7:1.

The SSI2140's transconductance cells and the exponential generator can be considered otherwise identical to the SSM2040. The SSI2140 also contains additional circuitry not found in the SSM2040:

- A on-chip "tempco" resistor with a typical value of 890Ω and a temperature coefficient of +3950ppm/°C. This resistor, functionally similar to the TelLabs Q81, can optionally be used to temperature compensate the q/kT factor of the exponential generator.
- An on-chip temperature compensated VCA designed for use in controlling the resonance ("Q") of a four pole low-pass filter configuration. The VCA's connections have been designed to allow multiple options for "Q compensation" which counteracts the effect increased Q has on the filter's DC gain. If the Q VCA isn't used for Q compensation it can be applied as a general-purpose VCA, for example as a high-pass filter.

Typical Application Circuit

Due to the SSI2140's wide range of function, Figure 1 shows only those connections common to virtually all applications. Later sections describe various filter configurations and design ideas for the Q VCA.

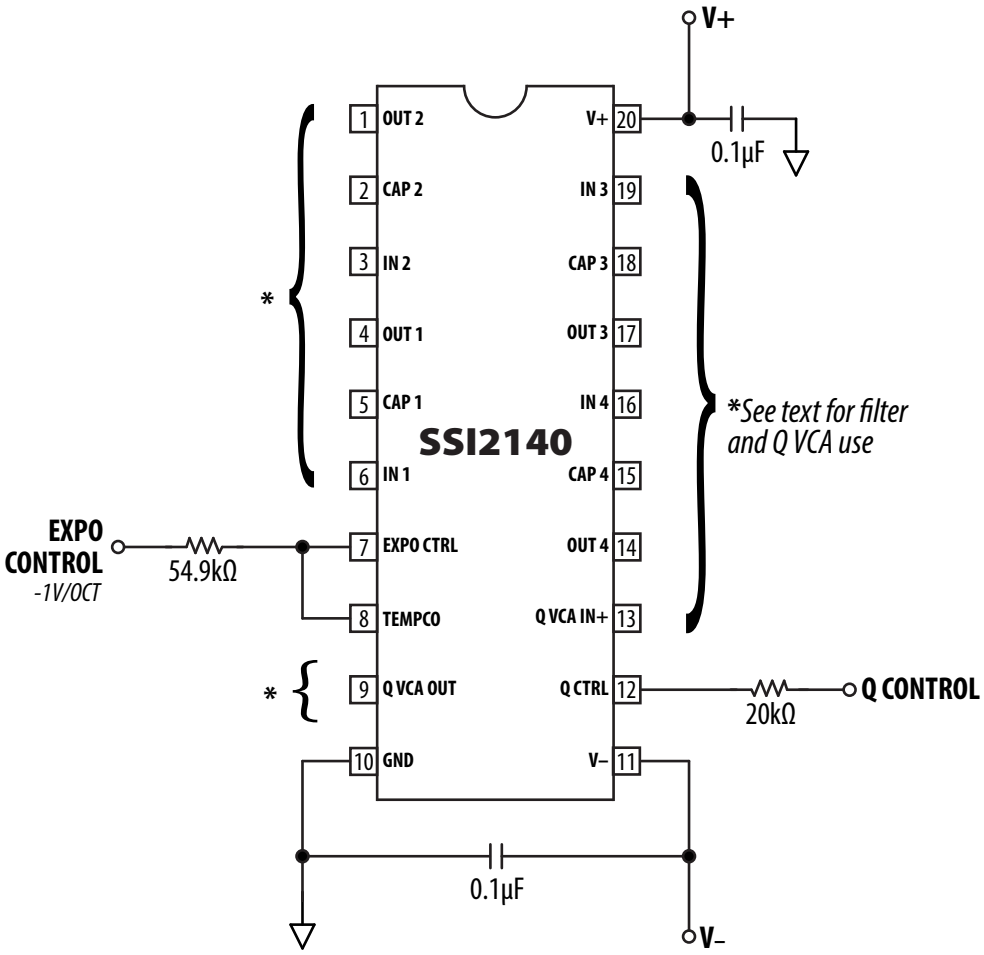


Figure 1: Common Connections for SSI2140
(Expo temperature compensation shown; see Figure 2 for uncompensated connection)

Power Supplies

The SSI2140 is normally powered from bipolar supplies ranging from ±4V to ±16V. Supplies should be locally bypassed with 100nF ceramic capacitors placed close to the supply pins and short traces to ground. It is also recommended to provide larger bulk decoupling caps on each board, typically 47µF to 100µF per rail.

Signal Inputs

The four transconductance cells have a very limited input range – beyond 40mV peak-to-peak (±20mV) the input stage starts to distort. The recommended input scheme is a 10kΩ resistor from the signal source to the input pin, and a 200Ω resistor to ground. This reduces the signal down to the tens of millivolts that the input can handle, and sets the recommended peak input signal to $2V_{P-P}$.

Higher input levels overdrive the input stage, resulting in a distortion that many will find desireable. See Unity-Gain Overdrive in the Applications section for managing overdrive.

Signal Outputs

The outputs of the transconductance cells are capable of driving 1V into a 5kΩ load. This is sufficient to drive the recommended 10kΩ feedback resistor and a 10kΩ input resistor to the next stage.

The Q VCA output is a current. If fed back to one of the transconductance cells, a direct connection can be made. For voltage output, a current-to-voltage converter op-amp is recommended as shown in the "Output Gain" compensated configuration of Figure 15.

Exponential Frequency Control

The frequency control pin has a typical sensitivity of -18mV per octave. It is recommended to use a series resistor together with a 1kΩ shunt resistor to attenuate external frequency control voltage down to this level. For example, for 1V per octave sensitivity use a 54.9kΩ series resistor and either an external 1kΩ shunt resistor or the internal tempco resistor giving a useful control range of +5V to -5V. See Figure 2.

Filter Capacitor Selection

For optimum audio performance use capacitors with low leakage and distortion. Ceramic C0G/NP0, polystyrene, and high-quality polyester types are recommended. The recommended value is 1nF. Smaller values will raise the cutoff frequency and larger values will lower it; for example, 470pF capacitors will approximately double the cut off frequency, while 2.2nF will halve it.

The smallest recommended value is 50pF, and care must be taken with parasitic capacitance and leakage. Larger capacitance values are also possible, but cost may become prohibitive.

Using the On-Chip Tempco Resistor

Pin 8 (TEMPCO) of the SSI2140 connects to an on-chip resistor whose other terminal is internally wired to ground. This resistor has a typical value of 890Ω and temperature coefficient of +3950ppm/°C. During normal operation, die temperature shifts the TEMPCO resistance to about 1kΩ (see page 10).

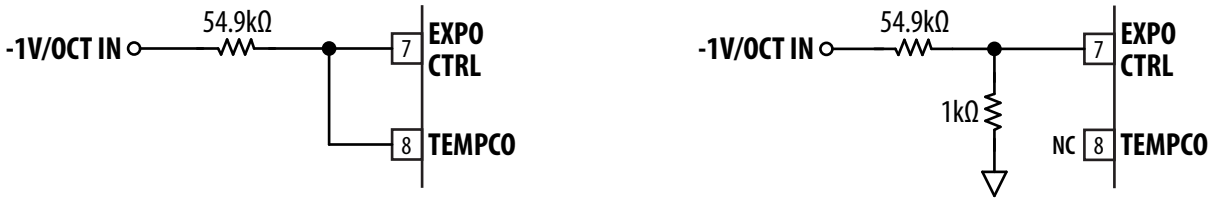
Using this as a resistive attenuator will temperature compensate the SSI2140 exponential generator's inherent gain factor of q/kT by multiplying the input voltage by a factor proportional to the die temperature T in degrees Kelvin. The value of the input series resistor for a 1V/octave response is 54.9kΩ as shown in Figure 1.

To take advantage of temperature compensation, simply tie pins 7 and 8 together. If the TEMPCO resistor is not used, pin 8 should be left open and a 1kΩ resistor added between pin 7 and ground to correctly scale the control voltage range. See Figure 2.

If two or more SSI2140s are used, for example a stereo synthesizer voice structure where two SSI2140s must track thermally, it is recommended to connect the internal compensation resistors in parallel. This arrangement will compensate for the average die temperature across the SSI2140s. Then the EXPO series resistor must be halved from 54.9kΩ down to 27.4k ohms. When more than two SSI2140s are connected in parallel the series resistor must be reduced accordingly.

Note this resistor, being an on-chip implementation, has certain characteristics that differ from discrete resistors:

- It has a wide tolerance, typically ±15%. An appropriate 1V/octave trim range must be implemented.
- It is slightly non-linear, resulting in a modest deviation from the accuracy achievable by the internal exponential generator alone. Specifically, lower input voltages corresponding to higher cutoff and resonant frequencies will lower the resistor value causing the pitch to be slightly flatter than expected. This effect should be less than a semitone.
- The voltage across the resistor (at pin 8) should not exceed +300mV, as this will forward bias the resistor with respect to its surrounding well and the resistor may draw excessive current. There is no need for such a voltage at this pin under normal application.



2a: *With On-Chip Temperature Compensation*

2b: *On-Chip Temperature Compensation Disabled*

Figure 2: TEMPCO Pin Connections

Resonance (Q) Control

The SSI2140 contains an internal current controlled amplifier that is temperature compensated for g_m. An external resistor turns this into a voltage controlled amplifier allowing easy scaling of control voltage range to Q control range. While this VCA has been designed and configured to control resonance of the filter in a four-pole low-pass configuration, its general purpose nature allows the creative designer great flexibility for other uses.

The Q VCA has a non-inverting low-level voltage input connected to pin 13 (Q VCA IN+) and a symmetric inverting input connected internally to the output of transconductance cell 4 by a 16:1 resistive divider. **If the Q VCA is not used, Q VCA IN+ and Q VCA Out pins should be grounded and the Q CNTL (pin 12) left open.**

The Q CNTL pin is a ground-referenced current input, with a range from 0µA (no resonance) to 500µA (maximum resonance). Oscillation will typically be observed at 222µA. For simple CV control a single resistor is needed; with the recommended value of 20kΩ a control voltage of 4.4V results in oscillation when used to control filter Q, and 0V equals zero resonance.

The transconductance of the VCA is typically 30µS/µA. The filter's loop gain is given by the following expression:

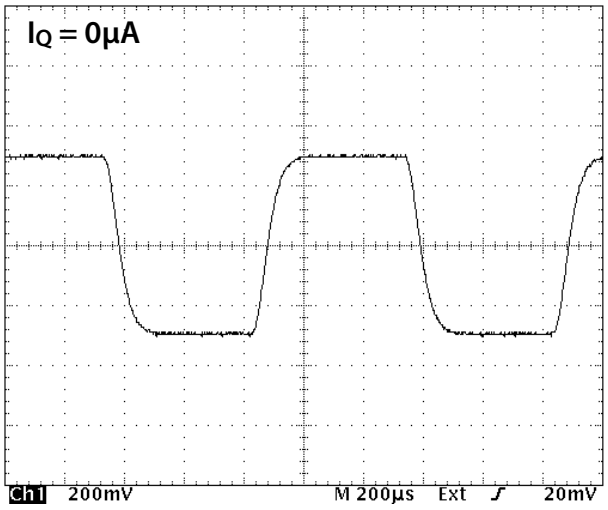
$$G_{Loop} = \frac{G_{VCAInput} K_{G_m} I_Q R_Q}{G_{FilterInput}}$$

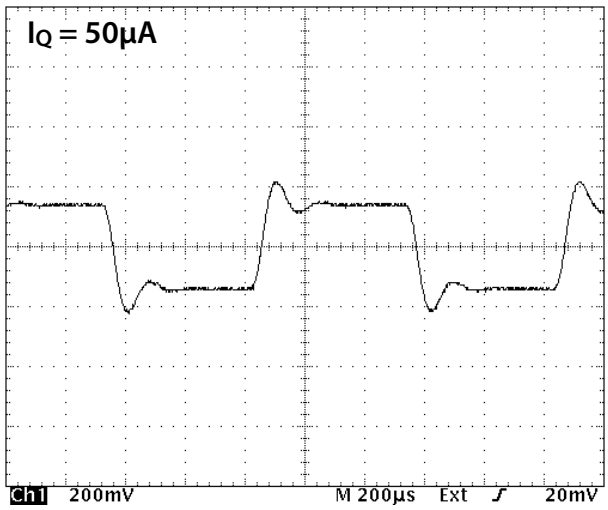
where G_{Loop} is the loop gain, $G_{FilterInput}$ is the gain of the resistive divider network at the filter input, $G_{VCAInput}$ is the gain of the resistive divider network at the VCA input, K_{gm} is the g_m constant of the VCA, I_Q is the VCA control current, and R_Q is the resistor on the output of the VCA (typically 200 Ohms). Re-arranging for I_Q we get the following expression:

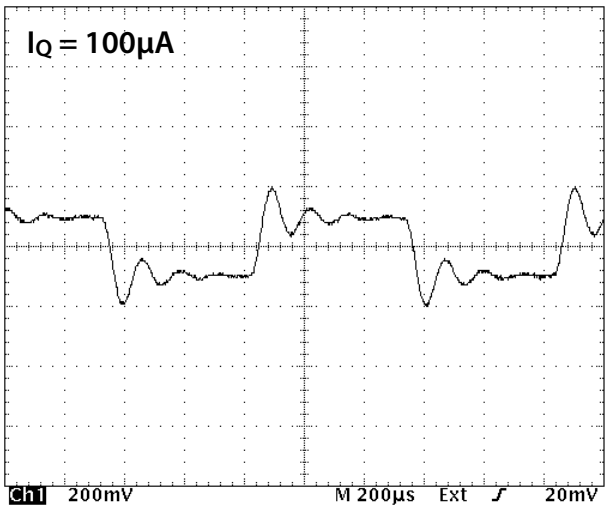
$$I_Q = \frac{G_{Loop} G_{FilterInput}}{G_{VCAInput} K_{G_m} R_Q}$$

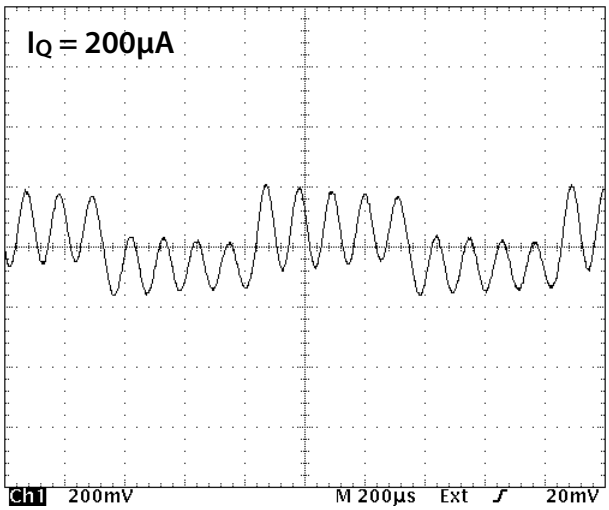
For oscillation, loop gain needs to be exactly 4.0 to compensate for the $\sqrt{2}$ attenuation per stage. The SSI2140 Q VCA has a 16:1 input attenuator. For the typical low-pass filter shown in Figure 3 the filter input attenuator is a 10k:200 resistor network, and R_Q is also the lower 200Ω resistor. Putting these figures into the above equation produces a VCA control current requirement of 222µA:

$$I_Q = \frac{4.000 \times \frac{200}{10k + 200}}{\frac{1k}{16k + 1k} \times 30 \times 200} = 222\mu A$$





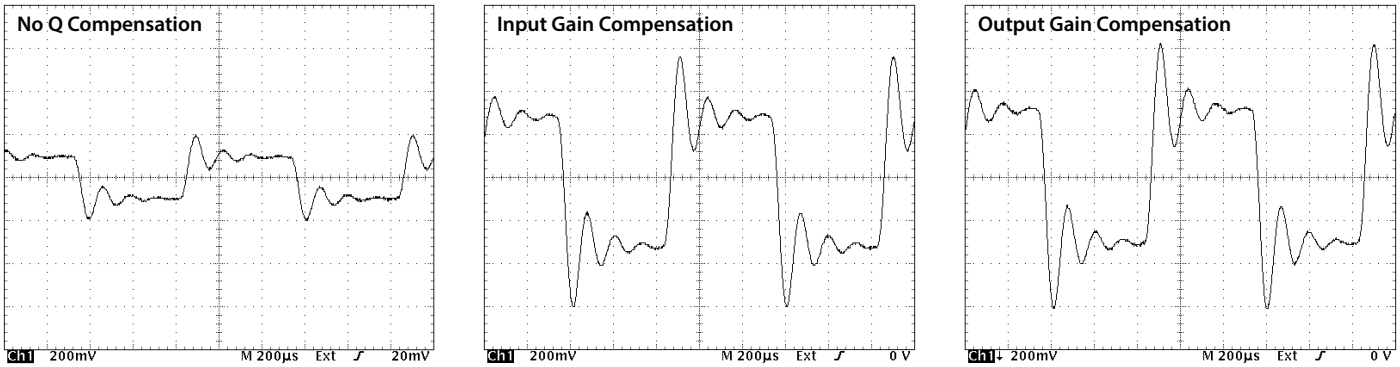




Plots on the previous page show a 1kHz 600mV$_{P-P}$ square wave signal applied to the circuit of Figure 3 against different Q control currents. Two points to note are that the overall amplitude drops as resonance increases, and when I_Q is 200µA the filter is very close to resonance.

Q Compensation

The arrangement of the Q circuit determines the type and degree of Q Compensation. Various configurations are described further in "Q Compensation." Plotted below are low-pass filter outputs for the two Q compensation schemes from a 1kHz square wave input and I_Q = 100µA. The no-compensation plot for the same I_Q is shown for comparison.



TYPICAL APPLICATION: FOUR-POLE LOW-PASS FILTER

A typical application of the SSI2140 is shown in Figure 3. The input signal (1V$_{P-P}$) is fed via a 10kΩ resistor into the first summing node. The reduced voltage across the 200Ω resistor is fed into the first transconductance cell's input pin. The voltage is then converted to a current according to the transconductance of the cell. Current flows into the 1000pF capacitor, producing a voltage which is buffered and provided at the output pin.

To construct a low-pass filter, a proportion of the output signal is fed back to the input. As the buffer is inverting, the output is of the opposite polarity to the input, and eventually the loop around the transconductance cell will stabilize according to the DC component of the input signal. This is the classic low-pass filter operation.

The output of the first stage is then fed into the next stage in exactly the same way, and so on for the remaining stages. The final output of the filter is taken from the output of the fourth transconductance buffer.

A proportion of the final output signal is also fed back to the input through the Q VCA. When the Q VCA is off, no signal is fed back to the input. As the Q VCA control voltage increases, an increasing amount of output signal is fed back to the input. At the cut off frequency the phase shift through each transconductance cell is 45 degrees, culminating in a total phase shift of 180 degrees. The output of the fourth stage then feeds into the inverting input of the Q VCA, giving a further 180 degrees phase shift. All together the 360 degrees phase shift enhances the output signal level at the cutoff frequency, giving rise to the classic peaking of the filter output.

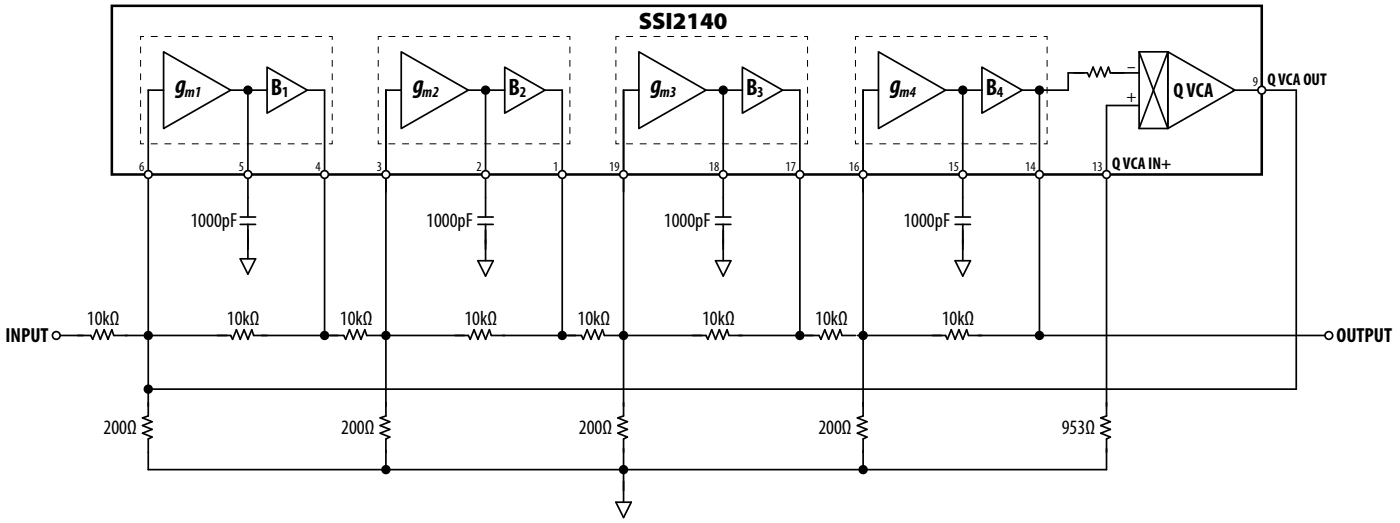


Figure 3: Four-Pole Low-Pass Filter with No Q Compensation

As the gain of the Q VCA is increased further the amount of feedback becomes sufficient to sustain oscillation of the filter. If amplitude control is implemented then it is possible to construct a low distortion sine wave oscillator whose frequency is controlled by the cutoff control. In this way it is possible to add an additional oscillator – albeit sine wave only – to a music synthesizer.

The configuration shown in Figure 3 is the simplest, and provides no Q compensation. As in the classic electronic music four-pole lowpass filter, the passband (DC) gain decreases with increasing Q proportional with the gain of the Q VCA. Near oscillation, the passband is attenuated by 12dB – an effect traditional synthesizer enthusiasts are accustomed to. Others prefer to avoid the passband attenuation effect, which is easily solved by the SSI2140's Q VCA as described in detail later in "Q Compensation."

PRINCIPLES OF OPERATION

The SSI2140 comprises four variable transconductance cells sharing a common control port, plus a temperature compensated current controlled variable gain amplifier.

Transconductance Amplifier

A simplified schematic of the transconductance cells is shown in Figure 4. Each cell comprises a variable transconductance amplifier followed by a high input-resistance buffer.

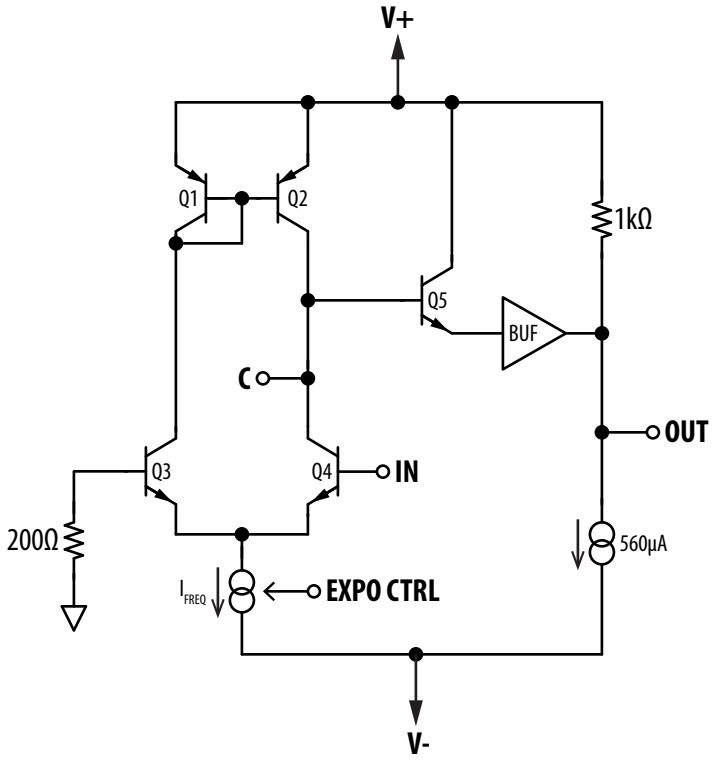


Figure 4: SSI2140 Simplified Circuit – Transconductance Cell and Buffer

Transistors Q1 and Q2 are a current mirror and provide an active load for the differential pair Q3 and Q4. The input to the transconductance amplifier is applied to the base of Q4. The base of Q3 is tied to ground through a 200Ω resistor.

When the input is 0V, both transistor bases are at the same potential so the same current flows through both Q3 and Q4. The total current, set by current source I_{FREQ} (controlled by the EXPO CTRL pin), is shared equally between Q3 and Q4. As $I_{FREQ}/2$ flows into the collector of Q3, by mirror action an equal but opposite current flows out of the collector of Q2. This current exactly balances the current flowing into Q4's collector, and so there is no current flowing into or out of the C terminal. Assuming a capacitor is connected to this terminal, the voltage across the capacitor does not change.

A small positive voltage applied to the base of Q4 causes it to pass more current according to Q4's transconductance. Because I_{FREQ} is held constant this results in less current flowing into Q3's collector. Action of the Q1/Q2 current mirror also reduces the current flowing out of Q2's collector. An imbalance causes a current to flow into the C pin, resulting in the voltage across the external capacitor falling at a constant rate, the slope of which is determined by the value of the capacitor and the magnitude of the current flowing out of the capacitor according to:

$$V_c = \frac{1}{C}\int i_c dt$$

where i_C is the output current of the transconductance cell, C is the value of the capacitor, and V_C is the voltage developed across the capacitor that is then buffered and provided at the output pin. For small negative voltages a similar operation occurs but in the opposite direction.

The ratio between the input voltage and output current ("g_m") is set by I_{FREQ}, which is controlled by a voltage on the EXPO CTRL pin. In a filter circuit this results in the cutoff frequency of each transconductance cell being adjustable over a wide range.

For best control feedthrough rejection the impedances seen by the bases of Q3 and Q4 must be the same. The base of Q3 is internally connected to GND through a 200Ω resistor, so the designer should aim to present a similar impedance to the base of Q4. The recommended circuit, with a 200Ω resistor to GND, satisfies this requirement; the effect of the 10kΩ input resistors is minimal.

Output Buffer

The voltage at the C pin is sensed by emitter follower Q5, before driving the buffer circuit BUF (the circuit inside the buffer is not shown). The output of BUF looks like a 1kΩ resistor to V+ and a 560µA current sink to V-. This results in an asymmetric output drive: the output can source up to 11.4mA (when V+ = +12V) but only sink up to 560µA.

Because the input signal is connected to the inverting input of the transconductance amplifier, and the output buffer is non-inverting, each transconductance cell inverts the input signal. This is important for pole mixing applications where the output is a weighted sum of the individual outputs.

Current Controlled Amplifier

The variable Q control is performed by a current-controlled amplifier shown in Figure 5.

The behavior of the current controlled amplifier is similar to the transconductance cells. Transistors Q1 and Q2 form a current mirror active load for differential transistor pair Q3 and Q4. The gain of the amplifier is set by the emitter currents which are set by the temperature-compensated current source. This current source is controlled by the externally-applied control current flowing into the ground-referenced Q CONTROL pin.

The Q VCA has two inputs. The non-inverting input, at the base of Q3, is connected to the Q VCA IN+ pin. The inverting input, at the base of Q4, is internally connected through a 16kΩ/1kΩ resistive divider, to the output of the fourth transconductance cell. Again, for minimal control feedthrough the impedances seen by both inputs should be the same.

The output current is taken from the junction between the collectors of Q2 and Q4. For correct operation this pin must be kept close to ground; for example a low value resistor or an op-amp I-to-V converter. If not required, it can be directly connected to ground.

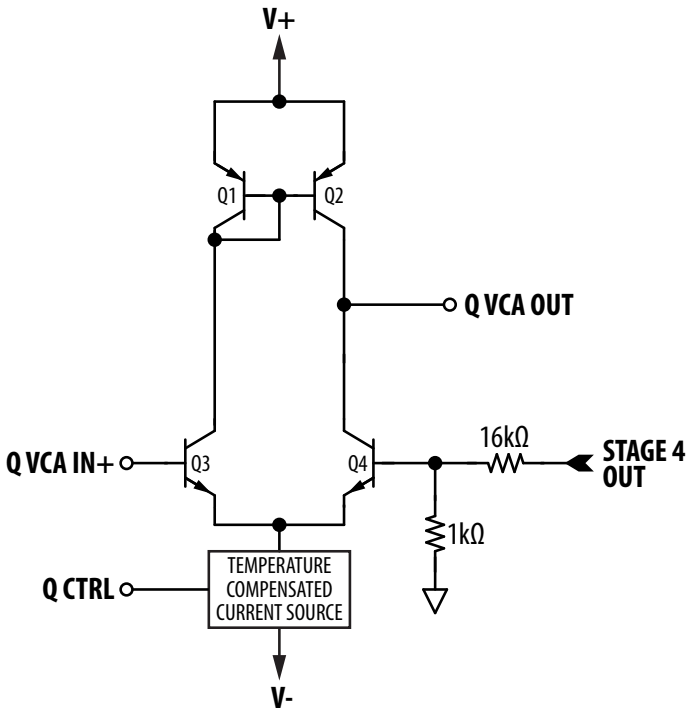


Figure 5: SSI2140 Simplified Circuit – Q VCA

Temperature Compensation

All semiconductor devices are sensitive to temperature. The SSI2140 includes three temperature compensation schemes. Firstly, the Q VCA automatically compensates for changes in the temperature of the IC, requiring no external connections. Secondly, the SSI2140 automatically compensates for the temperature variation of the transconductances of the four filter cells. Thirdly, an internal temperature-sensing element can be used to temperature-compensate the EXPO CTRL pin.

The compensation of the EXPO CTRL pin is provided by an internal 890Ω temperature-sensing resistor brought out to a pin adjacent to the EXPO CTRL pin and, together with a series resistor (54.9kΩ for 1V/oct), provides comprehensive temperature compensation. Its resistance at 25°C is typically 890Ω. However when the SSI2140 is powered the part dissipates around 120mW, heating up the silicon by about 20°C above ambient temperature. This increases the value of this resistor to about 1kΩ during normal operation, and which tracks the ambient temperature.

Temperature compensation of the EXPO CTRL pin is less useful in microprocessor-controlled polyphonic synthesizers, which may prefer to run regular tuning cycles to track temperature and keep all voices in tune together.

APPLICATION INFORMATION

FILTER DESIGN NOTES

Frequency control of all four SSI2140 transconductance cells is governed by the voltage at EXPO CTRL, which is described by:

$$G = 215\mu S \times 2^{\frac{-V_{EXPO}}{0.018}}$$

Filter Type	Figure	Gain (A)	F_c	Q	Transfer Function
Low-Pass - Real Pole	6	$\frac{-R2}{R1}$	$\frac{200G}{2\pi R2C}$	$\frac{1}{2}$	$\frac{-A}{(S+1)}$
High-Pass - Real Pole	7	1	$\frac{200G}{2\pi RC}$	$\frac{1}{2}$	$\frac{S}{(S+1)}$
All-Pass	8	1	$\frac{200G}{2\pi RC}$	$\frac{1}{2}$	$\frac{S-1}{(S+1)}$
Sallen & Key Low-Pass	9	$\frac{R2}{R1}$	$\frac{200G}{2\pi R2C}$	$\frac{R3}{2R4}$	$\frac{A}{(S^2+\frac{1}{Q}S+1)}$
Sallen & Key High-Pass	10	1	$\frac{200G}{2\pi R1C}$	$\frac{R2}{2R3}$	$\frac{S^2}{(S^2+\frac{1}{Q}S+1)}$
Sallen & Key Band-Pass	11	$\frac{-R2}{R1}$	$\frac{200G}{2\pi R2C}$	$\frac{R3}{2R2}$	$\frac{-AS}{(S^2+\frac{1}{Q}S+1)}$
State Variable Low-Pass	12	$\frac{-R2}{R1}$	$\frac{200G}{2\pi R3C}$	$\frac{R1(R4+R5)}{R5(2R1+R2)}$	$\frac{-A}{(S^2+\frac{1}{Q}S+1)}$
State Variable High-Pass		$\frac{-R2}{R1}$			$\frac{-AS^2}{(S^2+\frac{1}{Q}S+1)}$
State Variable Band-Pass		$\frac{R2}{R1}$			$\frac{AS}{(S^2+\frac{1}{Q}S+1)}$
Cauer (Elliptical)	13	$\frac{R2}{R1}$	$F_{Ca}=\frac{200G}{2\pi C1R2}$ $F_{Cb}=\frac{200G}{2\pi C2R2}$		$\frac{A(Sb^2+1)}{(Sa+1)^2(Sb+1)^2}$

The following Figures 6 through 13 illustrate many different filter configurations that are possible with the SSI2140. For each filter type, the table above gives the design equations for gain ("A"), cutoff frequency ("F_C"), resonance ("Q"), and the transfer functions in terms of "S", where $S = jf/F_C$. For the Cauer filter, there are two frequencies – F_a and F_b.

Three basic blocks – low-pass, high-pass and all-pass – comprise a single transconductance amplifier, a capacitor, and two or three resistors are shown in Figures 6 through 8, together with typical component values.

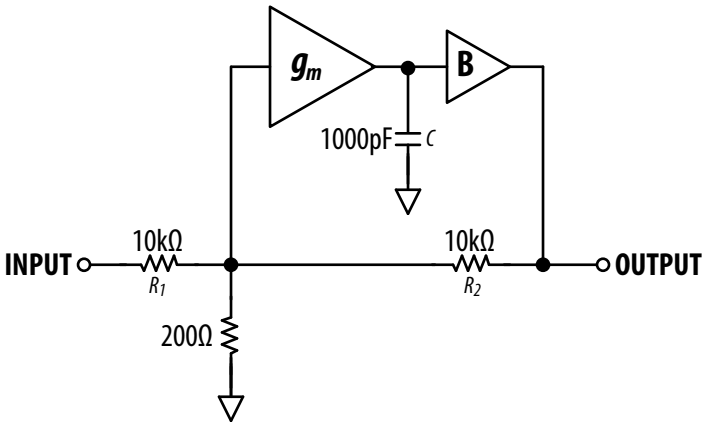


Figure 6: Basic Low-Pass Real Pole Circuit

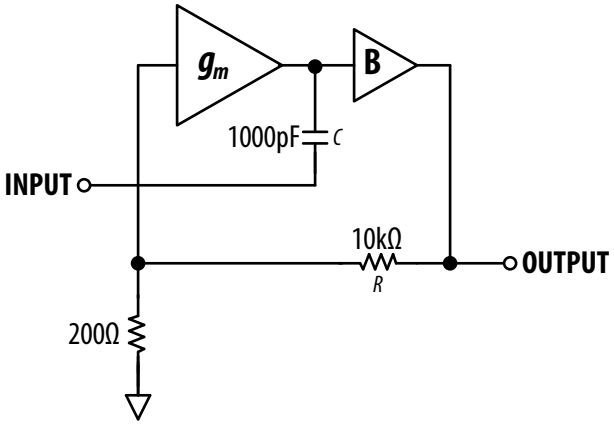


Figure 7: Basic High-Pass Real Pole Circuit

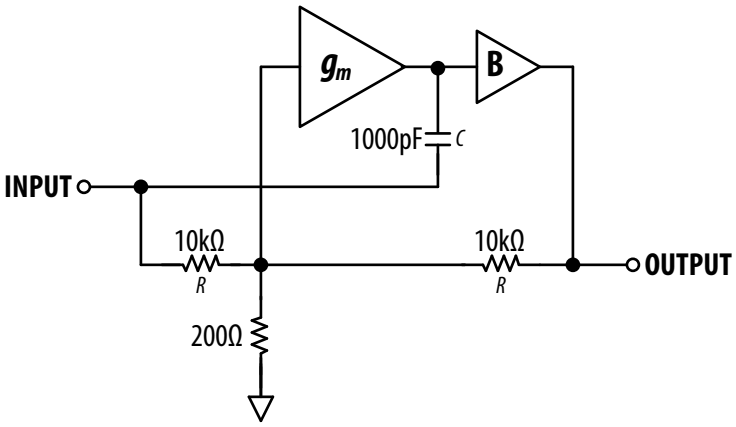


Figure 8: Basic All-Pass Circuit

More complex filter schemes are shown in Figures 9 through 12. Two of the most common filter topologies - Sallen and Key and KHN State Variable - are easily realized with the SSI2140 by using two transconductance amplifiers together with an external op-amp.

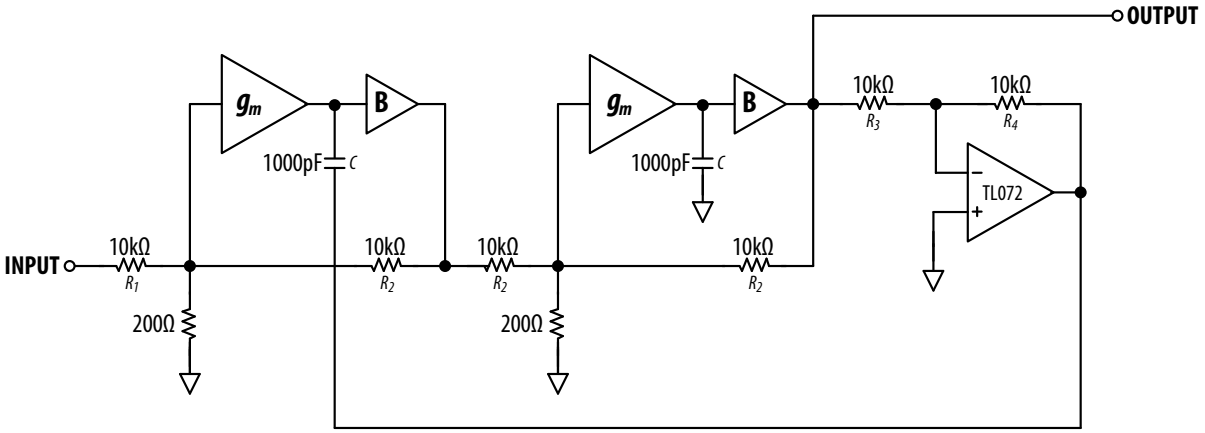


Figure 9: Sallen and Key Low-Pass Filter

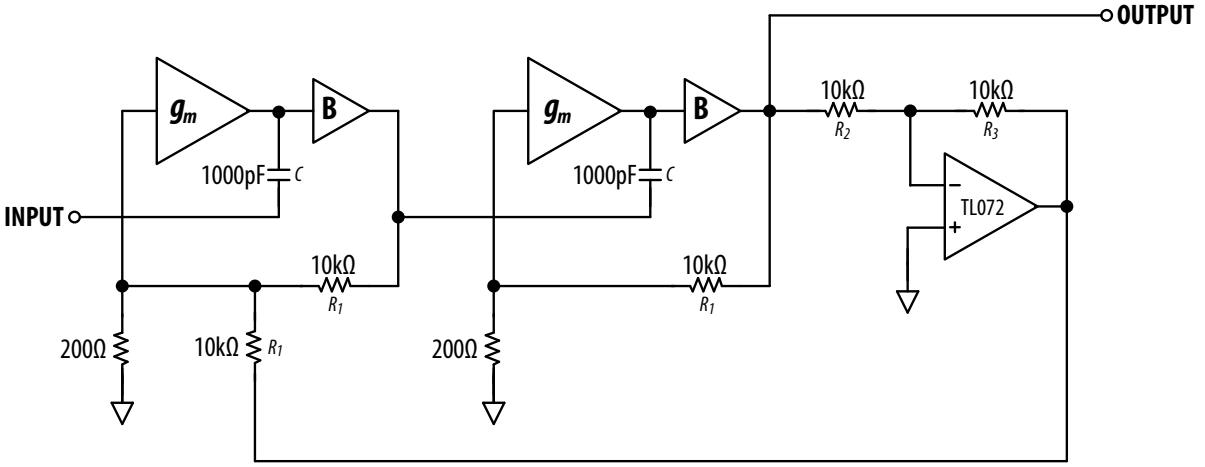


Figure 10: Sallen and Key High-Pass Filter

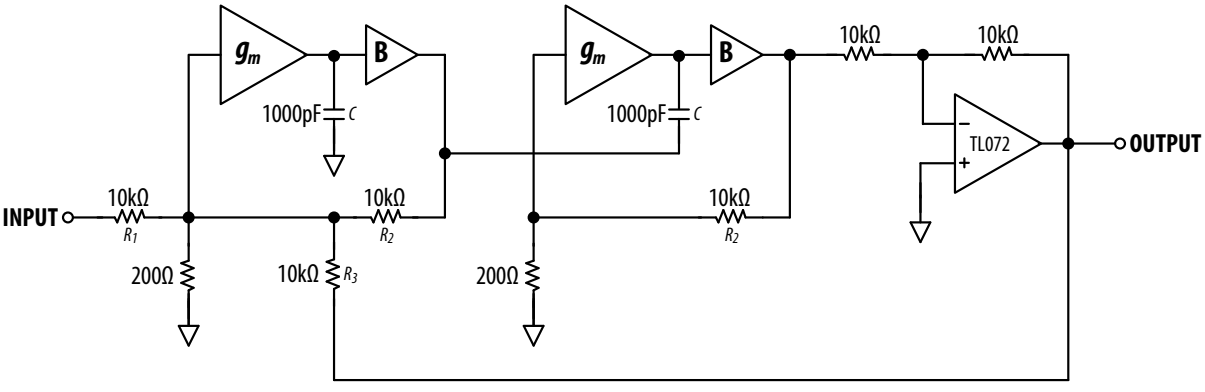


Figure 11: Sallen and Key Band-Pass Filter

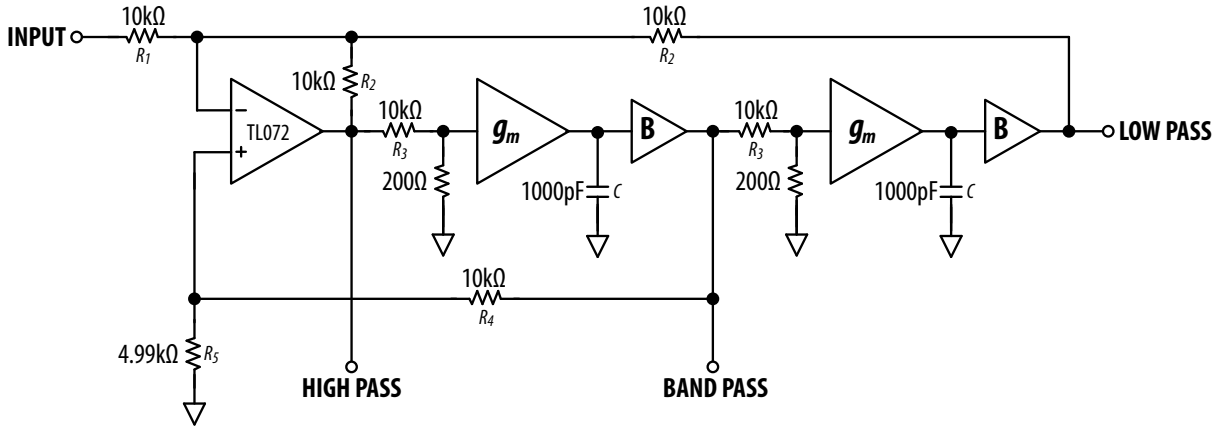


Figure 12: State Variable Filter

In order for the State Variable to behave according to the design equations, the parallel combination of R4 and R5 must equal the parallel combination of R1 and R2/2. In algebraic terms:

$$\frac{R4R5}{R4+R5} = \frac{R1R2}{2R1+R2}$$

A final example is the Cauer, or Elliptical, filter (Figure 13) giving equalized ripple in the pass and stop bands, and very sharp transition between the passband and stopband. This type is typically used in a DAC reconstruction filter where the sharp cutoff is very close to the ideal brickwall filter needed to get the output bandwidth as close to the Nyquist frequency as possible without sacrificing too much of the high-frequency content.

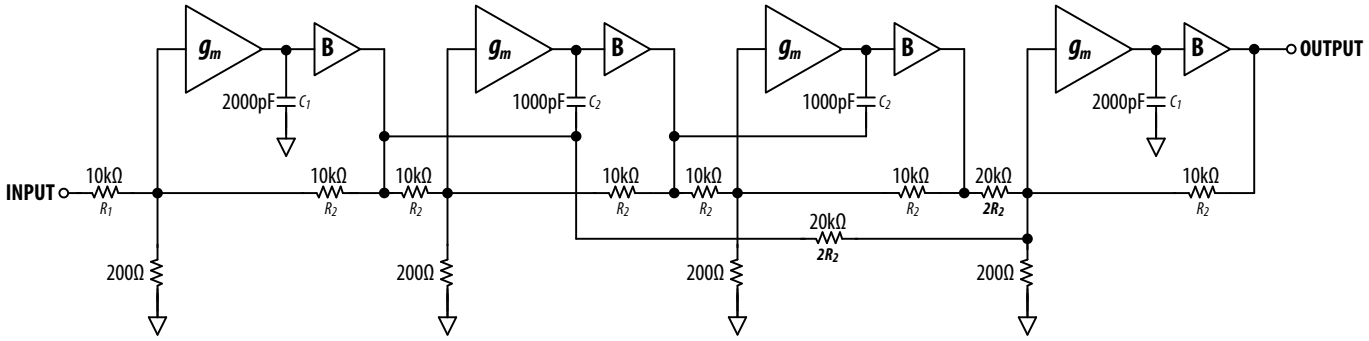


Figure 13: Cauer (Elliptical) Filter

Q COMPENSATION

The topology of the Q control circuit determines the type and degree of Q Compensation. Three alternatives are presented. For purposes of clarity the control inputs (Frequency and Q) are not shown as they remain the same in all configurations – see Figure 1. If Q compensation is not required, it is possible to use the SSI2140 to implement two filters with a common frequency control, such as a stereo filter or two tracking filters for interesting filter curves.

"Classic" Uncompensated Filter

The configuration of Figure 3 is the simplest, and provides resonance control with no Q compensation. As in the original electronic music four-pole low-pass filter, the passband (DC) gain decreases with increasing Q proportional with gain of the Q VCA. Near oscillation, the passband is attenuated by 12dB.

Input Gain Compensation

The "Input Gain" compensated configuration of Figure 14 provides Q compensation by feeding the signal input into the positive input of the Q VCA. Thus as the Q increases, more signal is applied to the filter, compensating for the increased negative feedback through the Q VCA. With the values shown, the passband gain remains constant with varying Q. Changing the values of R_{QI} and R_{QG} allows the designer to tailor the degree of Q compensation to the particular application. These resistors can also be made variable in real-time by use of a potentiometer or an appropriate VCA. For best Q control rejection, select R_{QI} to be 16.2kΩ and R_{QG} to 1kΩ to match the internal network.

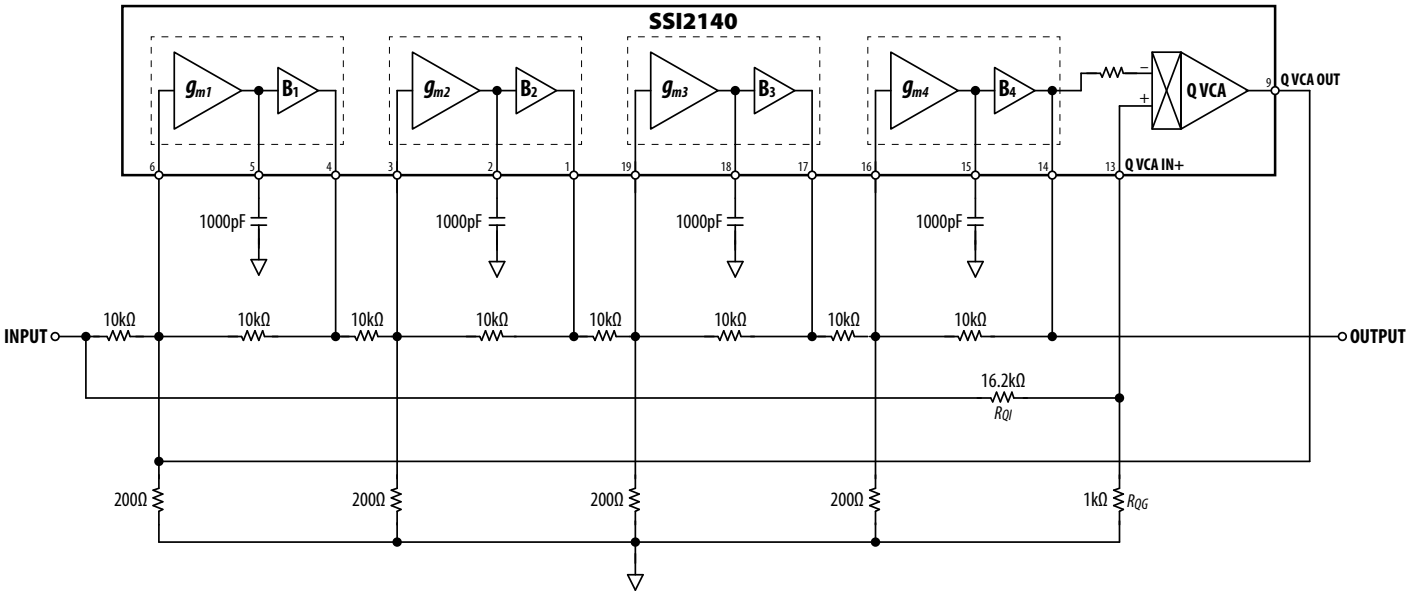


Figure 14: "Input Gain" Q Compensation

Output Gain Compensation

The "Output Gain" compensated configuration of Figure 15 adds compensating gain to the filter core's output to form the final output. In contrast to Input Gain compensation, the core filter signal level is not altered by Q compensation. This provides less distortion at high Q's resulting in a somewhat different timbre when Q compensation is applied. With the values shown, the passband gain remains constant with varying Q. As above, the various resistor values can be changed to tailor the degree of Q compensation and distortion to the particular application, and can also be made variable in real-time by use of potentiometers or appropriate VCAs.

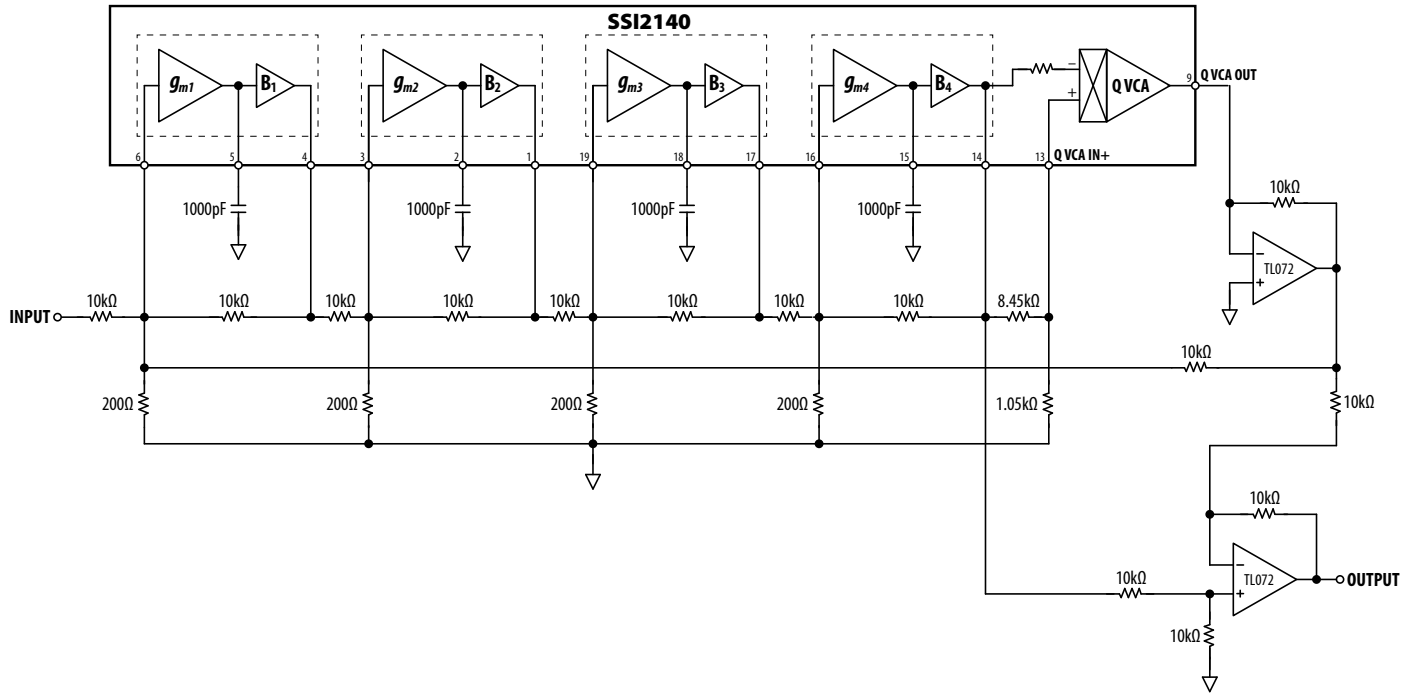


Figure 15: "Output Gain" Q Compensation

Q-COMPENSATION SWITCHING

As described above there are three possible Q compensation schemes for the SSI2140: none, input gain, and output gain. In many applications the designer will choose one scheme for their application. But with a two-pole three-way switch it is possible to manually choose which scheme is used during operation. See Figure 16.

The two poles of the switch set where the Q VCA's input and output go. In the uncompensated setting (position 1), the non-inverting Q VCA input is terminated to ground, and the Q VCA output connects directly back to the first input pin. In the input gain setting (position 2) the Q VCA input is connected to the AUDIO IN signal source, while the Q VCA output remains in the same position as for the uncompensated scheme. Note that in both these settings the output of the upper op amp is held at ground and so the AUDIO OUT is a buffered version of the final output (pin 14).

In the output gain setting (position 3), the Q VCA input comes from the final g_m cell output (pin 14), but at a higher level than the internal signal path resulting in the Q VCA producing a non-inverted output. This is then inverted by the upper op amp and fed both to the input g_m cell and to the output differential amplifier, similar to that shown in Figure 15.

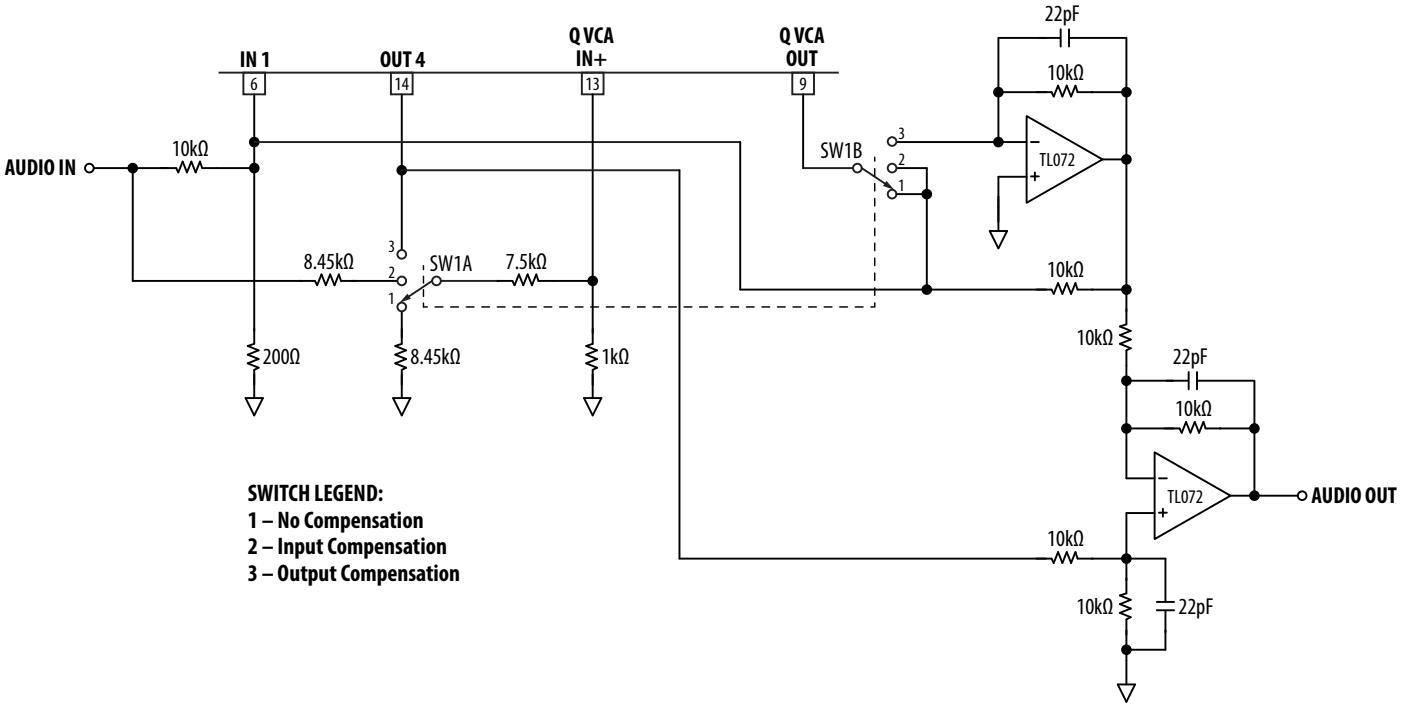


Figure 16: Q Compensation Mode Switching

IMPLEMENTING OTHER FUNCTIONS WITH THE Q VCA

The Q VCA can be used for a variety of signal processing functions. This section outlines some useful applications, including a triangle oscillator and a classic form of voltage-controlled filter. Note that in some cases the correct operation requires the fourth transconductance cell to be disabled as shown in the figures.

Voltage-Controlled Triangle Oscillator

Often it is desirable to modulate a filter's cutoff frequency. Using the well-known Miller integrator/Schmitt trigger configuration the Q VCA easily creates a voltage-controlled triangle oscillator. Figure 17 shows one such circuit.

The control current is set by the external control voltage and resistor (pin 7; see Figure 1). The output current of the Q VCA is accumulated by the op amp integrator. Capacitor C is chosen to match the desired range of operation. For most applications a FET input opamp and good quality integrating capacitor are recommended; for example, a TL072 opamp and C0G/NP0 or polystyrene capacitor.

The triangle output feeds into a Schmitt trigger based around the LM311 comparator. The diodes clamp the output signal to plus/minus one diode drop about ground, and the 10kΩ and 4.99kΩ resistors bias the diodes. The 10kΩ and 16kΩ resistors on the input to the LM311 provide the necessary hysteresis, and set the amplitude of the triangle wave to about $2V_{P-P}$. The 16:1 resistor network on the input to the Q VCA provides the recommended input matching.

The linear control relationship of the Q VCA results in the triangle oscillator having a linear volts-per-Hz control response. If an exponential volts-per-octave response is required then an external exponential converter is required (e.g., SSI2164).

Oscillation frequency is given by the following equation (assuming 2V swing, and 0.6V diode voltage):

$$F = \frac{0.265 \times V_{CTRL}}{R_{CTRL} \times C} Hz$$

For example, if the maximum control voltage is 5V for a target frequency of 1kHz and using a 10nF capacitor, then by rearranging this equation into:

$$R_{CTRL} = \frac{0.265 \times V_{MAX}}{C \times F_{MAX}} ohms$$

suggests a value of 132kΩ. The nearest standard value of 130kΩ gives a maximum frequency of 1020Hz.

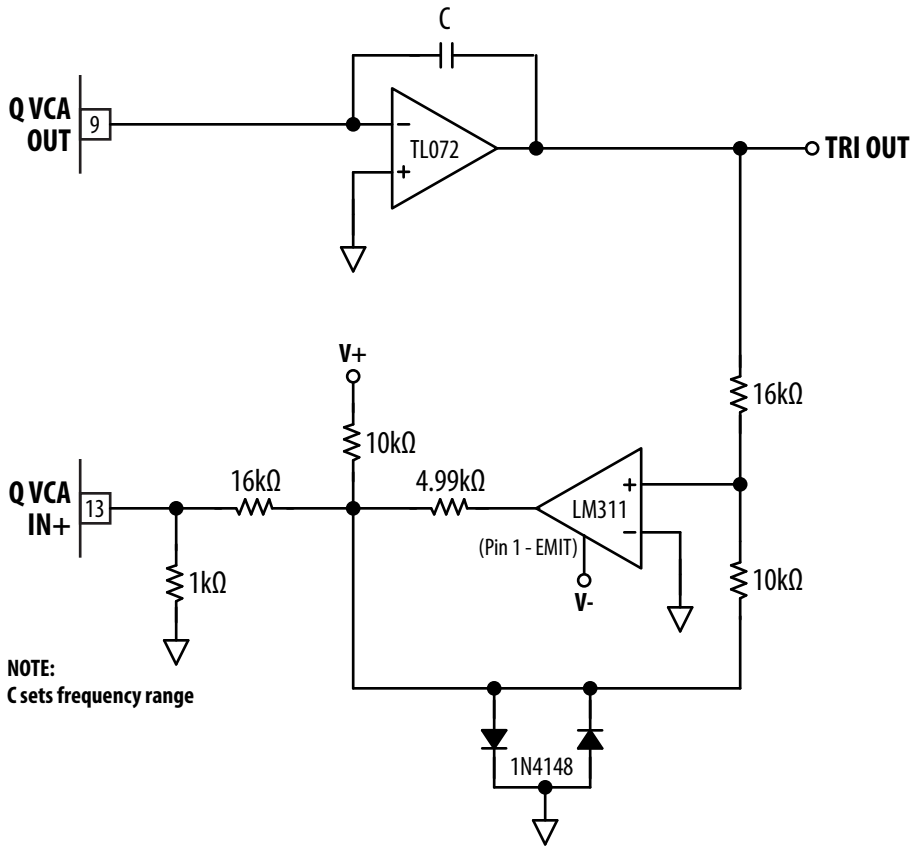


Figure 17: Q VCA as Triangle Oscillator

Implementing Filters With The Q VCA

The Q VCA may be used to implement a single-pole voltage-controlled filter. The 4th g_m cell is disabled by connecting pins 14, 15 and 16 to ground. An example single-pole high-pass filter, based on Dennis Colin's US patent 3,805,091, is shown in Figure 18. With minor changes it is also possible to implement low-pass and all-pass filters.

The input signal is reduced by the 10k/R divider, with the aim of keeping the peak signal level at the op amp's non-inverting input to below ±300mV. The high-pass filter is comprised of the capacitor C and the effective resistance of the Q VCA, set by the 16:1 input network and the control current into pin 12.

UNITY-GAIN OVERDRIVE

The input stage of the SSI2140 can only be driven to a few mV above and below zero for minimal distortion. However, it is possible to drive the input harder for classic overdriven filter distortion effects. This results in asymmetrical soft-clipping of the signal in the first transconductance cell, producing even-order harmonic content that is considered pleasing to the ear and part of the original SSM2040's appeal.

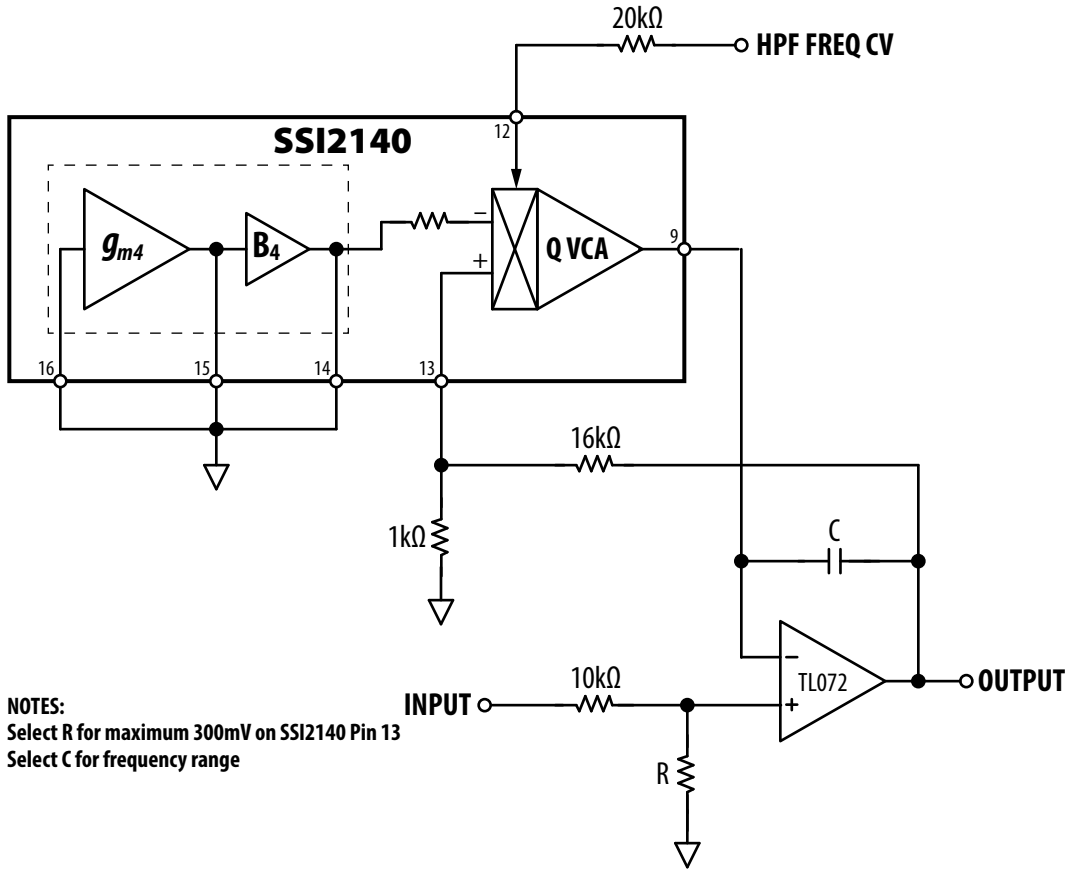


Figure 18: Q VCA as a Voltage-Controlled High-Pass Filter

With the addition of two gain cells from an SSI2164 (or both halves of an SSI2162) it is possible to add voltage-controlled unity-gain variable distortion around the SSI2140. See Figure 19.

Starting with a standard SSI2140 four-pole low-pass filter (the uncompensated version is shown for clarity but this technique is applicable to the compensated versions as well) a voltage-controlled amplifier increases the signal drive into the input of the first transconductance cell. With the DRIVE at 0V the gain of the input SSI2164 VCA is 0 dB. The inverting buffer opamp ensures a sensible positive DRIVE control range.

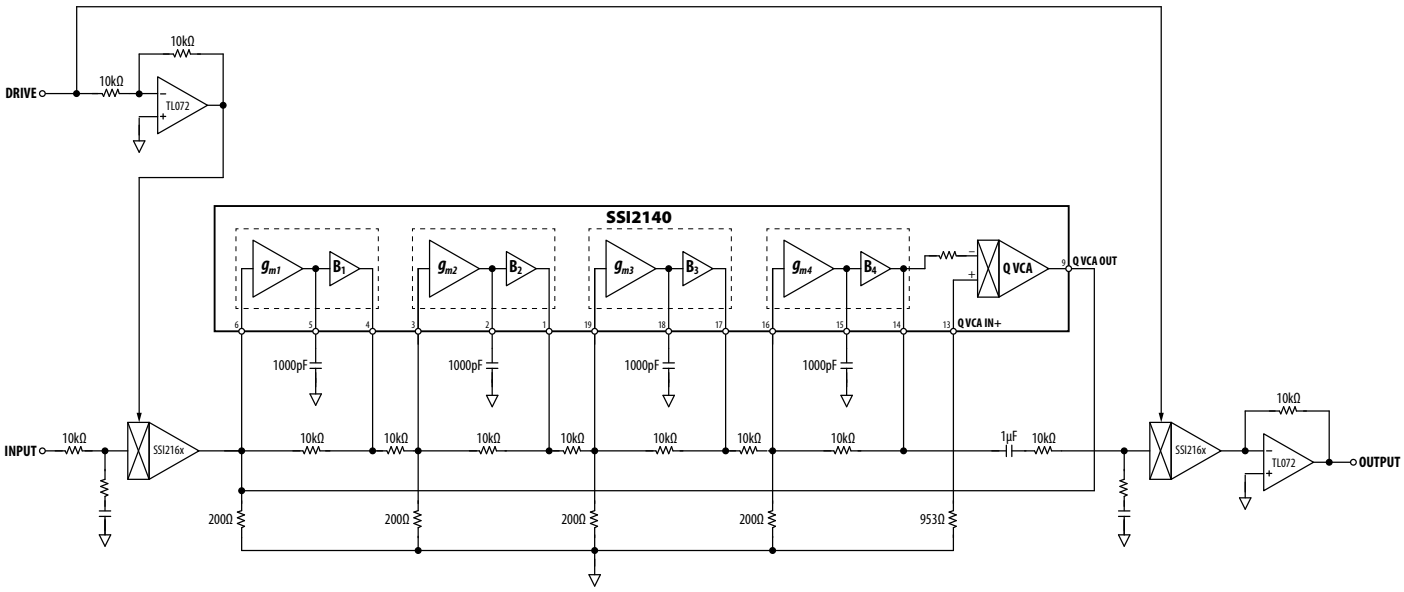


Figure 19: Unity Gain Overdrive

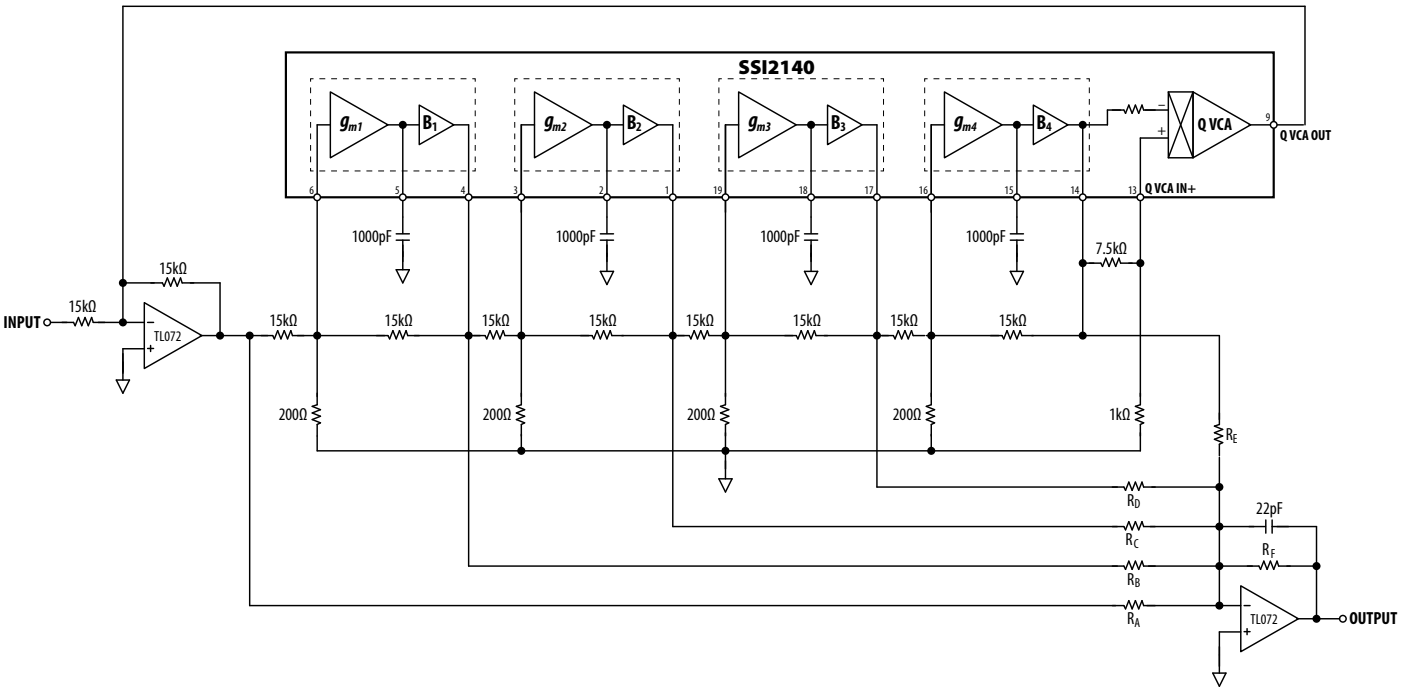


Figure 20: Pole-Mixing Multi-Mode Filter

As the DRIVE is increased to around +300mV, corresponding to a gain of +10dB, with a $1V_{P-P}$ input signal the SSI2140 starts to distort. If DRIVE is increased further, say to +600mV, the SSI2164 amplifies the input signal by +20dB (10x) and the SSI2140 produces significant even-order harmonic distortion. The second SSI2164 gain cell corrects the level of the output signal. As the gain of the first VCA increases, the second VCA attenuates the output of the filter.

This technique is limited to input signals with well-defined levels - ideal for synthesizers where the filter is placed immediately after the oscillator. At low signal levels significant gain would be needed to overdrive the input of the SSI2140. The SSI2164 is limited to about +20dB of gain which is best used with the SSI2140 for creating exceptional overdriven distortion effects.

MULTI-MODE POLE MIXING

The SSI2140 in its classic form provides four cascaded low-pass filter sections. While it is possible to construct other filter types (refer to Filter Design Notes), these configurations are fixed at the design stage.

However, it is well known that this basic form together with a multi-channel mixer can implement many different filter types simply by mixing different amounts of the intermediate outputs (corresponding to the filter's poles in the s-domain) together. This can be done with weighted resistors and analog switches. This technique is discussed in detail in the section MULTI-MODE FILTERS of Sound Semiconductor's separate Application Note AN701, with Table 1 giving the mixing ratios to get many different filter types.

The same technique can be used with the SSI2140 as its transconductance cells invert the phase of the signal in the same way as SSI2164-based low-pass filters. Using the same naming scheme as in AN701 the circuit of Figure 20 can implement a wide range of filter types.

For correct operation the input and output resistors have been scaled up to keep the minimum load seen by the buffer outputs to 5kΩ or more. This also requires the pole mixing resistors to be 15kΩ or greater, and for the designer to scale the mixer feedback resistor to produce the correct gains. For example, for the "1LP 2HP 1AP" filter mode the gains for taps A to E are 0, 1, 4, 5 and 2 respectively. The highest gain is 5, which sets the feedback resistor R_F to 75kΩ. From this the remaining resistors can be calculated: R_A = open-circuit, R_B = 75kΩ, R_C = 18.75kΩ, R_D = 15kΩ, and R_E = 37.5kΩ.

The first pole tap 'A' must include the resonance feedback signal. To achieve this an op amp mixes the input signal and the phase-corrected output of the Q VCA. If input Q compensation is required this can be achieved in the same way as shown in Figure 14 with the addition of a 16.2k resistor from the signal input to the Q VCA's non-inverting input.

Note that for this type of filter it is very important to follow the advice in AN701; primarily, choosing tight tolerance components for the resistors and filter capacitors for optimum performance.

FOUR-STAGE PHASER

This section presents a four-stage phaser effect complete with voltage-controlled modulation generator.

The phaser comprises four all-pass filter sections (Figure 21) in series. Each section adds a 90-degree phase shift at the frequency set by the EXPO CTRL pin. Frequencies either side of the cutoff frequency shift smoothly from 0 to 180 degrees. The output of the all-pass filter chain is then mixed with the original signal to generate the sharp notches that produce the characteristic phaser sound.

The modulator is based on the voltage-controlled triangle oscillator originally shown in Figure 17, with values adjusted for low frequency operation. Since the fourth g_m cell is used in this application an additional 16kΩ resistor feeds in an opposing amount of the signal into the non-inverting input of the VCA to cancel out the internally-routed signal.

In the circuit of Figure 21 the modulating frequency of the triangle oscillator is set by a manual "RATE" control but could also be controlled by another voltage source giving variable phasing frequency; for example, an envelope follower could change the phasing rate with the level of the input signal with quiet audio slowly phased and loud audio rapidly phased.

The circuit shown has fixed depth and no resonance path. To adjust the depth of the phasing effect place an attenuator on the output of the final all-pass filter (a manual level control or a VCA). Likewise, for resonance feed a fraction of the output of the final all-pass filter back to the input of the first all-pass filter, again either through a manual control or another VCA. An SSI2162, with its two VCAs, would be ideal for this application.

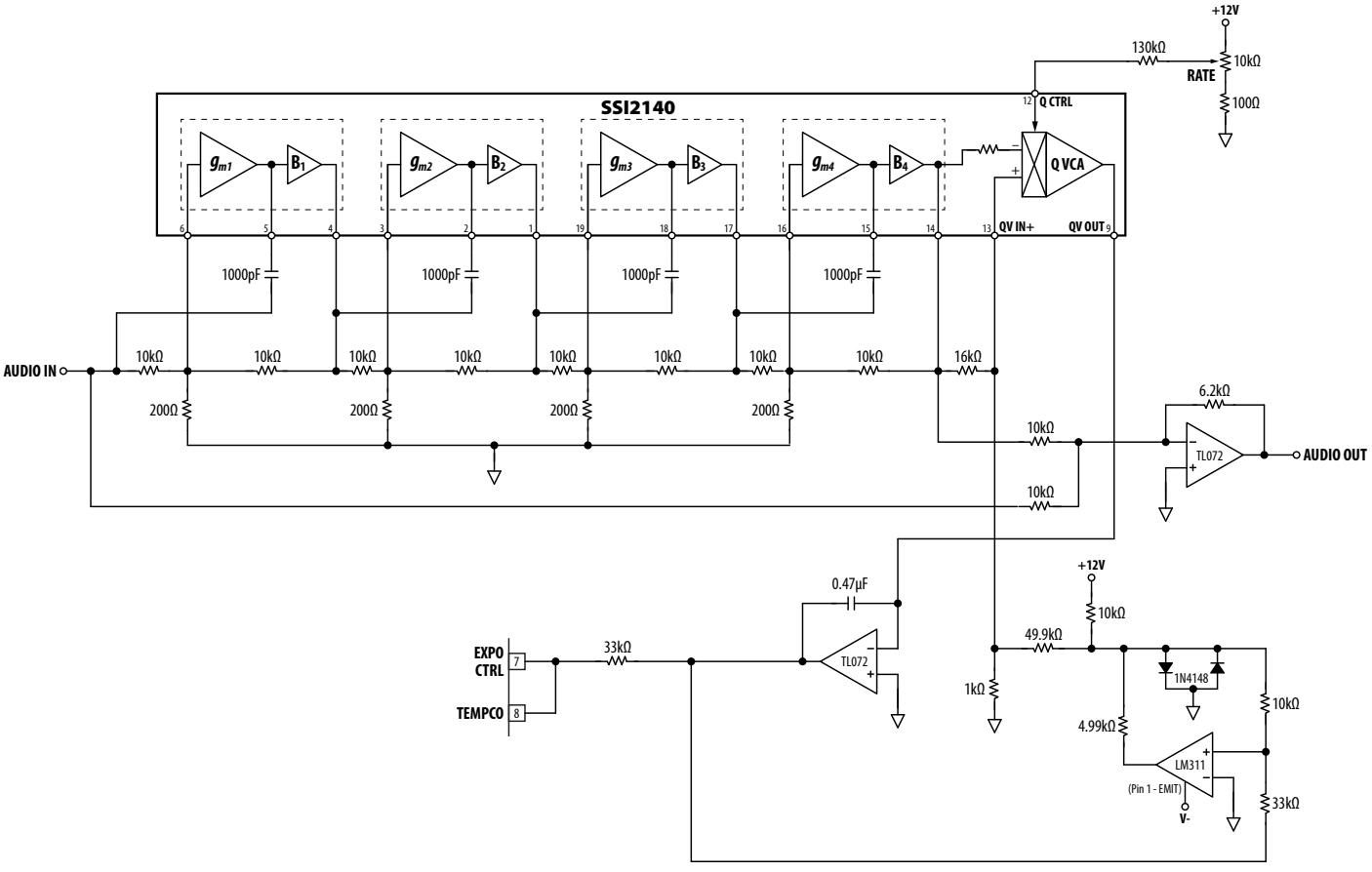
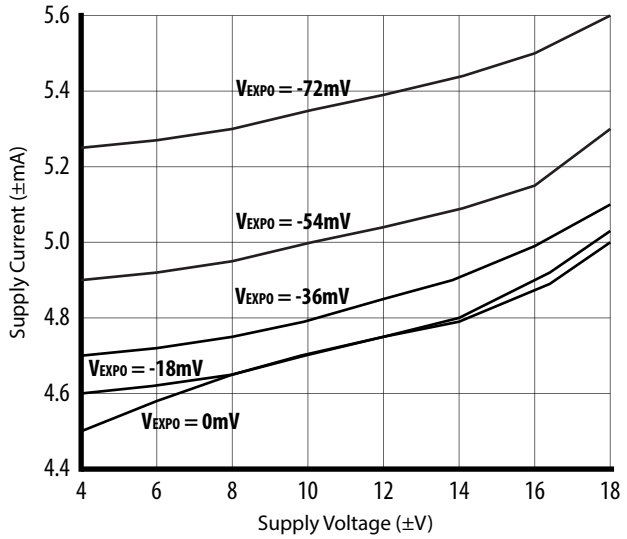


Figure 21: Four-Stage Phaser-Modulator

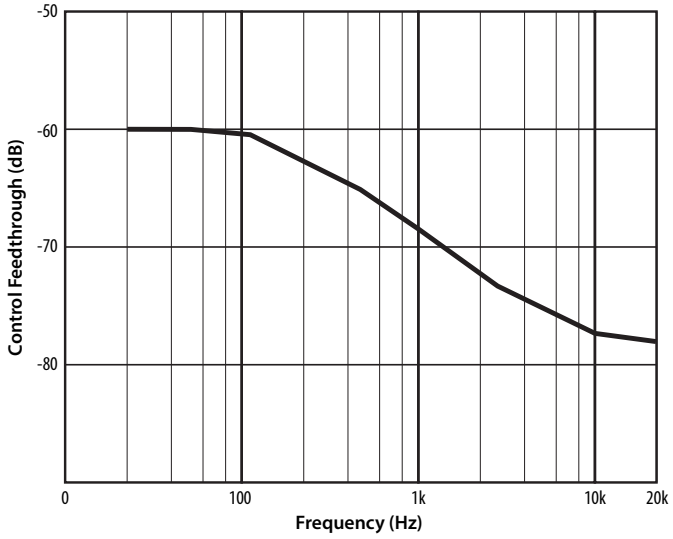
TYPICAL PERFORMANCE GRAPHS

Figure 3 Application Circuit using Fig. 2a on-chip Tempco at V_S = ±12V, I_{QCNTL} = 0µA, f = 1kHz; unless otherwise noted.



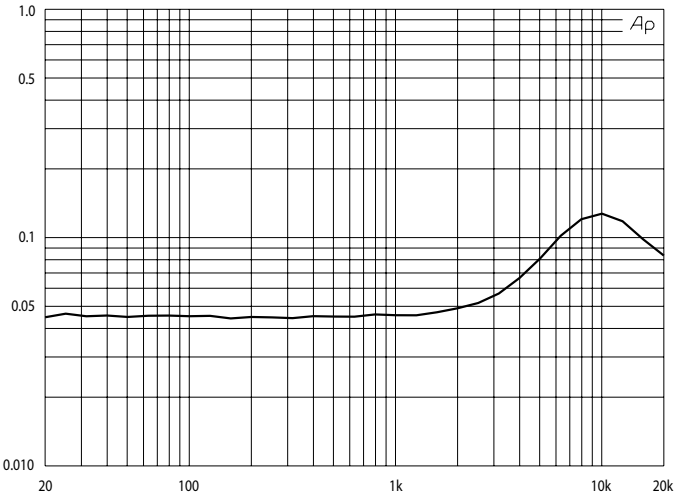
Supply Current vs. Supply Voltage and EXPO Voltage

V_{IN} = 1V_{P-P} sinewave; V_{EXPO} signal applied at pin 7.



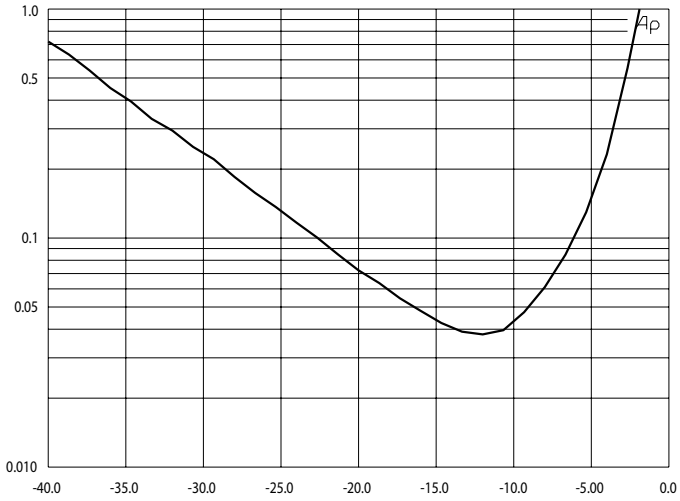
Control Feedthrough vs. Frequency

V_{EXPO} = 36mV_{P-P} sinewave applied at pin 7; V_{IN} = GND



THD+N (%) vs. Frequency (Hz)

Figure 14 Application Circuit, V_{IN} = -10dBu, V_{EXPO} = -100mV; 20Hz to 80kHz Filter



THD+N (%) vs. Amplitude (dBu)

Figure 14 Application Circuit, f = 1kHz, V_{EXPO} = -100mV; 10Hz to 22kHz Filter

DESIGN SUPPORT

Sound Semiconductor provides the following design tools for the SSI2140, which are available from Sound Semiconductor and its authorized resellers:

A versatile evaluation board with the SSI2140 configured for low-pass operation. Select one to four poles and all three Q compensation modes; controls for cutoff frequency, resonance (Q), and input overdrive, with optional temperature compensation. 3.5mm audio input and output jacks make interfacing with existing audio equipment easy. Pin headers support more detailed experimentation.

EVB2140LPR1-B *(SSI2140 only)*
EVB2140LPR1-P *(Fully populated)*

A low cost DIP adaptor board with mounted SSI2140. Ideal for developing prototypes without resorting to SMT assembly.

DAB2140